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| UNIVERSITY OF INFORMATION TECHNOLOGY  **COMPUTER ENGINEERING DEPARTMENT** | **FINAL EXAMINATION I (2019-2020)**  **COURSE: DEGITAL LOGIC DESIGN**  *Time duration: 60 minutes*  *(Paper materials are not allowed)*  *(OEP Students do the test by English,*  *Regular Students do the test by Vietnamese)*  *(Students need only do PART 1,*  *PART 2 has been done on class)* |

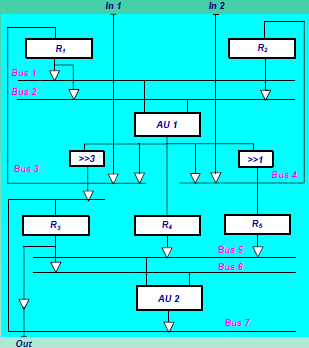
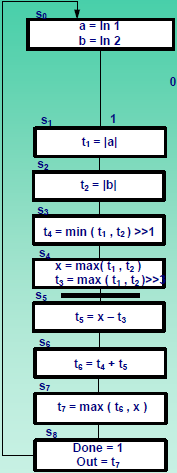
**PART 1: PAPER TEST (3 points)**

# Question 1: (1.5 points)

1. What is the multiple cycle design? Describe the disadvantages and advantages of multiple cycle design?
2. What is the pipelined functional unit design? How does the pipelined functional unit design improve the performance compared with the non-pipelined functional unit design?

# Question 2: (1.5 points)

Given the datapath pipelined design and its ASM for Square Root Approximation (SRA) calculation as below:

Where, R1 = [a, t1], R2 = [b, t2], R3 = [t3, t5, t6, t7], R4 = [x], R5 = [t4]

AU1 = [abs/min/max], AU2 = [+/-/max]

1. Explain benefits of the datapath pipelined design?
2. If there are 100 pairs of inputs (in1, in2), how many cycles are needed to calculate the SRA for these 100 pairs of inputs with above datapath pipelined design?

**PART 2: COMPUTER TEST**

# Question 3 (3 points)

Design RTL circuit for Square Root Approximation (SRA) using functional-unit sharing. Two shared functional-unit groups, which are (abs/max) and (abs/min/+/-) are used to design.

# Question 4 (4 points)

Design RTL circuit for Square Root Approximation (SRA) using datapath with pipelined functional unit.

**This examination’s learning outcomes (LO) (matching to subject syllabus’s LO)**

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| **Question** | **LO** | **Description** |
| 1 | G4 | Ability to comprehend professional materials |
| 2 | G2 | Ability to know analyze the cost and latency of the circuits, use ASM and FSMD models in the design process |
| 3 | G1 | Ability to analyze finite state machine circuits, data paths, and control units*.* |
| 4 | G2 | Ability to to optimize the circuits use ASM and FSMD models in the design process |

**Approved by Head of Subject Designed by**